FLEX 10K Power Consumption

TECHNICAL BRIEF 23 June 1997

Altera® FLEX® 10K devices combine the flexibility of programmable logic with the density and efficiency of embedded gate arrays. They offer these features through their unique architecture, which includes both a logic array and an embedded array. The logic array and the I/O pins communicate through the high-speed FastTrack™ Interconnect routing structure, a series of continuous horizontal and vertical routing channels that traverse the device. This technical brief discusses the fast and power-efficient interconnect structure of the FLEX 10K architecture.

Power Consumption

When evaluating power consumption, it is important to use comparable operating conditions. For example, at first glance Xilinx XC4000 devices may appear to consume less power than Altera FLEX 10K devices. However, Xilinx calculates power dissipation using a counter benchmark in which a configurable logic block (CLB) drives only its neighboring CLB. The power dissipation calculated with this method is significantly less than in typical designs. In typical designs, CLBs are scattered, and a CLB's flipflop drives more than just the neighboring CLB. In contrast, Altera uses a more conservative approach to calculate power dissipation by assuming that a FLEX 10K logic element (LE) drives an entire row interconnect channel, not just part of it. Thus, when using the same operating conditions, FLEX 10K and XC4000 device power consumption is similar.

Table 1 shows the power consumption of FLEX 10K and XC4000 devices of comparable density and under similar operating conditions.

Table 1. FLEX 10K & XC4000 Power Consumption *Note (1)*

Device	Power Consumption (W)	
	Operating Frequency = 10 MHz	Operating Frequency = 30 MHz
XC4025E	1.0	3.0
XC4028EX	1.1	3.2
XC4036EX	1.4	4.1
EPF10K30	1.0	3.1
EPF10K40	1.5	4.4

Note:
(1) Data was compiled by Altera Applications.

Table 2 shows the data used to calculate the power dissipation of XC4025E, XC4028EX, and XC4036EX devices.

Table 2. XC4000 Device Information *Note (1)*

	XC4025E	XC4028EX	XC4036EX
One CLB's flipflop driving its neighbor plus 9 interconnect segments	0.2 mW/MTps, *Note (2)*	0.2 mW/MTps, *Note (2)*	0.2 mW/MTps, *Note (2)*
One global clock driving all CLB flipflops	40 mW/MHz	40 mW/MHz, *Note (3)*	50.6 mW/MHz, *Note (4)*
One full-length Longline with one driving CLB source and one driven CLB load	0.24 mW/MTps	0.24 mW/MTps, *Note (3)*	0.30 mW/MTps, *Note (5)*
Number of Longlines	256	512	576

Notes:

(1) Source: Xilinx *The Programmable Logic Data Book*, September 1996, page 13-12.
(2) MTps = million transitions per second.
(3) Because the XC4028EX and XC4025E devices have the same number of CLBs, Altera conservatively assumes that the XC4028EX global clock consumes the same power as the XC4025E global clock. Similarly, an XC4028EX Longline consumes the same power as an XC4025E Longline.
(4) Because the XC4036EX has 1,296 CLBs, its global clock power dissipation is estimated by scaling from the XC4025E: (40 mW / MHz) × (1,296 CLBs) / (1,024 CLBs).
(5) Because the XC4036EX device has 1,296 CLBs, the power dissipation of each of its Longlines is estimated by scaling from the XC4025E: (0.24 mW / MTps) × (1,296 CLBs) / (1,024 CLBs).

In an effort to compare the power consumption of FLEX 10K and XC4000 devices under similar operating conditions, Altera Applications derived a couple of power equations. The first power equation can be used to calculate the power consumed by the Xilinx XC4025E, XC4028EX, and XC4036EX devices using a 30-MHz clock frequency, 16-bit counters, all Longlines in the device, and a 12.5% switching rate.

$$\text{Power} = (M \times C \times \mathbf{tog_{LC}} \times \mathbf{f_{MAX}} \times P_{CLB}) + (G \times \mathbf{f_{MAX}} \times P_{CLK}) + (L \times \mathbf{tog_{LC}} \times \mathbf{f_{MAX}} \times P_{LL})$$

Where:
- M = Number of flipflops per CLB
- C = Number of CLBs
- $\mathbf{tog_{LC}}$ = Switching rate
- $\mathbf{f_{MAX}}$ = Maximum clock frequency
- P_{CLB} = Power to frequency ratio of the CLB driver
- G = Number of global clocks
- P_{CLK} = Power to frequency ratio of the global clock
- L = Number of Longlines
- P_{LL} = Power to frequency ratio of the longlines

XC4025E = (2 FF/CLB × 1,024 CLBs × 12.5% × 30 MHz × 0.2 mW/MTps) + (1 Global Clock × 30 MHz × 40 mW/MHz) + (256 Longlines × 12.5% × 30MHz × 0.24 mW/MTps)
= 2,966 mW

XC4028EX = (2 FF/CLB × 1,024 CLBs × 12.5% × 30 MHz × 0.2 mW/MTps) + (1 Global Clock × 30 MHz × 40 mW/MHz) + (512 Longlines × 12.5% × 30 MHz × 0.24 mW/MTps)
= 3,197 mW

XC4036EX = (2 FF/CLB × 1,296 CLBs × 12.5% × 30 MHz × 0.2 mW/MTps) + (1 Global Clock × 30 MHz × 50.6 mW/MHz) + (576 Longlines × 12.5% × 30 MHz × 0.30 mW/MTps)
= 4,110 mW

The following power equation can be used to calculate the power consumed by the Altera EPF10K30 and EPF10K40 devices when using a 30-MHz clock frequency and a 12.5% switching rate. Data for these equations was obtained from *Application Note 74 (Evaluating Power for Altera Devices)* and the *FLEX 10K Embedded Programmable Logic Family Data Sheet*.

$$\text{Power} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times V_{CC}$$

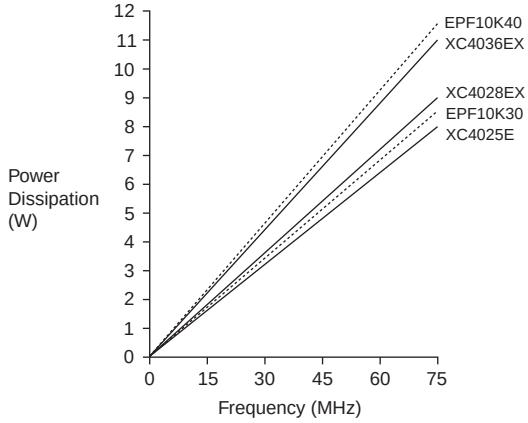
Where:
- K = Constant
- $\mathbf{f_{MAX}}$ = Maximum clock frequency
- N = Number of LEs
- $\mathbf{tog_{LC}}$ = Switching rate
- V_{CC} = Supply voltage

$$\text{EPF10K30} = 97 \times 30\ \text{MHz} \times 1{,}728\ \text{LEs} \times 12.5\% \times 5\ \text{V}$$
$$= 3{,}143\ \text{mW}$$

$$\text{EPF10K40} = 101 \times 30\ \text{MHz} \times 2{,}304\ \text{LEs} \times 12.5\% \times 5\ \text{V}$$
$$= 4{,}363\ \text{mW}$$

Figure 1 compares the power consumed by XC4000 and FLEX 10K devices.

Figure 1. FLEX 10K & XC4000 Power Dissipation



FastTrack Interconnect Structure

Signal interconnections within FLEX 10K devices are provided by the FastTrack Interconnect routing structure, a series of fast, continuous row and column channels that run the entire length and width of the device. This global routing structure provides predictable performance, even in complex designs.

The high speed of the FastTrack Interconnect routing structure is achieved through the low resistance and capacitance of its continuous channels. These channels are driven by CMOS buffers, which are not pre-charged.

Competing devices use a segmented interconnect structure, which is slower due to the high resistance and capacitance of the pass transistors that connect the segments. Under conditions found in typical designs, the high resistance and capacitance of segmented interconnect structures increase power consumption and reduce performance.

References

The documents listed below provide more detailed information. Part numbers are in parentheses.

- *FLEX 10K Embedded Programmable Logic Family Data Sheet (A-DS-F10K-02)*
- *AN 74: Evaluating Power for Altera Devices (A-AN-074-01)*

You can request these documents from:

- Altera Literature Services at (888) 3-ALTERA
- World-wide web site at **http://www.altera.com**
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